REMARKS

The following remarks are fully and completely responsive to the Office Action dated September 11, 2003. In the outstanding Office Action, claim 20 was rejected under 35 U.S.C. § 102(b). No new matter has been added. Claim 20 is presented for reconsideration.

35 U.S.C. § 102(b)

Claim 20 was rejected under 35 U.S.C. § 102(b) as being anticipated by Kocis et al. In making this rejection, the Office Action asserts that this reference teaches each element of the claimed invention. Applicant respectfully disagrees and requests reconsideration.

Claim 20 recites a variable delay circuit. This circuit includes a first delay circuit having a plurality of first delay stages connected in cascade and receiving an input signal at the initial stage of the first delay stages. A second delay circuit having a plurality of second delay stages identical to the first delay stages is connected in cascade and receives a first timing signal at the initial stage of the second delay stages. A detecting circuit receives a second timing signal asynchronous to the first timing signal, and detects, of delayed timing signals outputted from each of the second delay stages, a delayed timing signal having a transition edge near to a transition edge of the second timing signal. A selecting circuit selects a delayed signal output from the first delay stage corresponding to the second delay stage outputting the delayed timing signal detected by said detecting circuit.

The variable delay circuit in Kocis et al. has a different configuration than the present invention. As a result, Kocis cannot achieve the same effect achieved by the present invention. The detecting circuit in Kocis et al. receives the calibration clock and its delayed signal (the synchronous signal of the calibration clock). Thus, the signals received by the detecting circuit in Kocis et al. (flip-flops 114-1, 114-N) do not correspond to the first and the second timing signals in the present invention that are asynchronous to each other. As shown in Fig. 24, for example, the delay time of the variable delay circuit can be set to the time difference between the transition edge of the first timing signal CLKA (Fig. 21), which is generated in synchronization with the clock signal CLK, and the transition edge of the second timing signal RTIM4 (p.34, lines 16-18 in the Specification), which is generated asynchronous to the clock signal CLK.

Therefore, Kocis et al. fails to teach and/or suggest each and every element of the claimed invention. Specifically, Kocis et al. fails to teach and/or suggest a detecting circuit receiving a second timing signal asynchronous to the first timing signal, and detecting, of delayed timing signals outputted from each of said second delay stages, a delayed timing signal having a transition edge near to a transition edge of the second timing signal. Therefore, Applicant respectfully requests reconsideration and withdrawal of the rejection of claim 20 under 35 U.S.C. § 102(b).

Conclusion

Applicant's remarks have overcome the rejection set forth in the Office Action dated September 11, 2003. Specifically, Applicant's remarks have distinguished claim 20 from Kocis et al. and thus overcome the rejection of this claim under 35 U.S.C. § 102(b).

Accordingly, claim 20 is in condition for allowance. Therefore, Applicant respectfully requests reconsideration and allowance of claim 20.

Applicant submits that the application is now in condition for allowance. If the Examiner believes that the application is not in condition for allowance, Applicant respectfully requests that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

In the event this paper is not timely filed, Applicant hereby petitions for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment to Deposit Account No. 01-2300, referring to client-matter number 108397-00067.

Respectfully submitted,

Rustan J. Hill
Registration No. 37,351

Customer No. 004372
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W., Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810

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